

# DATA SHEET

## **TDA8785**

**8-bit high-speed analog-to-digital  
converter with gain and offset  
controls**

Preliminary specification  
File under Integrated Circuits, IC02

1996 Jan 17

# 8-bit high-speed analog-to-digital converter with gain and offset controls

## TDA8785

### FEATURES

- 8-bit analog-to-digital converter (ADC)
- 8-bit digital-to-analog converter (DAC)
- Sampling rate up to 30 Msps for both ADC and DAC
- Binary or two's complement 3-state TTL outputs
- TTL compatible inputs and outputs
- 100 MHz variable gain amplifier (0 to 20 dB) externally controlled
- All analog inputs and outputs are differential (can also be used in single-ended format)
- Analog input signal from 0.1 to 1.0 V (p-p) differential
- Offset amplifier with:
  - slow offset control ( $\pm 250$  mV)
  - fast offset control ( $\pm 500$  mV) eventually driven by internal DAC
- ADC output code of 8 (typ.) when analog input signal and offset correction inputs are 0 V

- Gain, slow offset control inputs and DAC output swing of 1.5 V (p-p) range ( $2.75 \pm 0.75$  V)
- 2.75 V reference voltage
- Internal references for ADC and DAC.

### GENERAL DESCRIPTION

The TDA8785 is an 8-bit analog-to-digital converter with gain and offset controls for the input signal. An internal 8-bit DAC provides digital adjustment of the different input offsets.

### APPLICATIONS

- CCD type of systems
- Scanner
- Copier
- Video acquisition.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CCA1}$	analog supply voltage 1		4.75	5.0	5.25	V
$V_{CCA2}$	analog supply voltage 2		4.75	5.0	5.25	V
$V_{CCD}$	digital supply voltage		4.75	5.0	5.25	V
$V_{CCO}$	TTL output supply voltage		4.75	5.0	5.25	V
$I_{CCA}$	analog supply current		–	80	–	mA
$I_{CCD}$	digital supply current		–	30	–	mA
$I_{CCO}$	TTL output supply current		–	9	–	mA
INL	integral non-linearity	0 to 20 dB gain; ramp input	–	$\pm 0.7$	tbf	LSB
DNL	differential non-linearity	0 to 20 dB gain; ramp input	–	$\pm 0.4$	tbf	LSB
$f_{clk(max)}$	maximum clock frequency	ADC and DAC	30	–	–	MHz
B	controlled gain amplifier bandwidth		–	100	–	MHz
$P_{tot}$	total power dissipation		–	600	–	mW

### ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8785H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2

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## BLOCK DIAGRAM

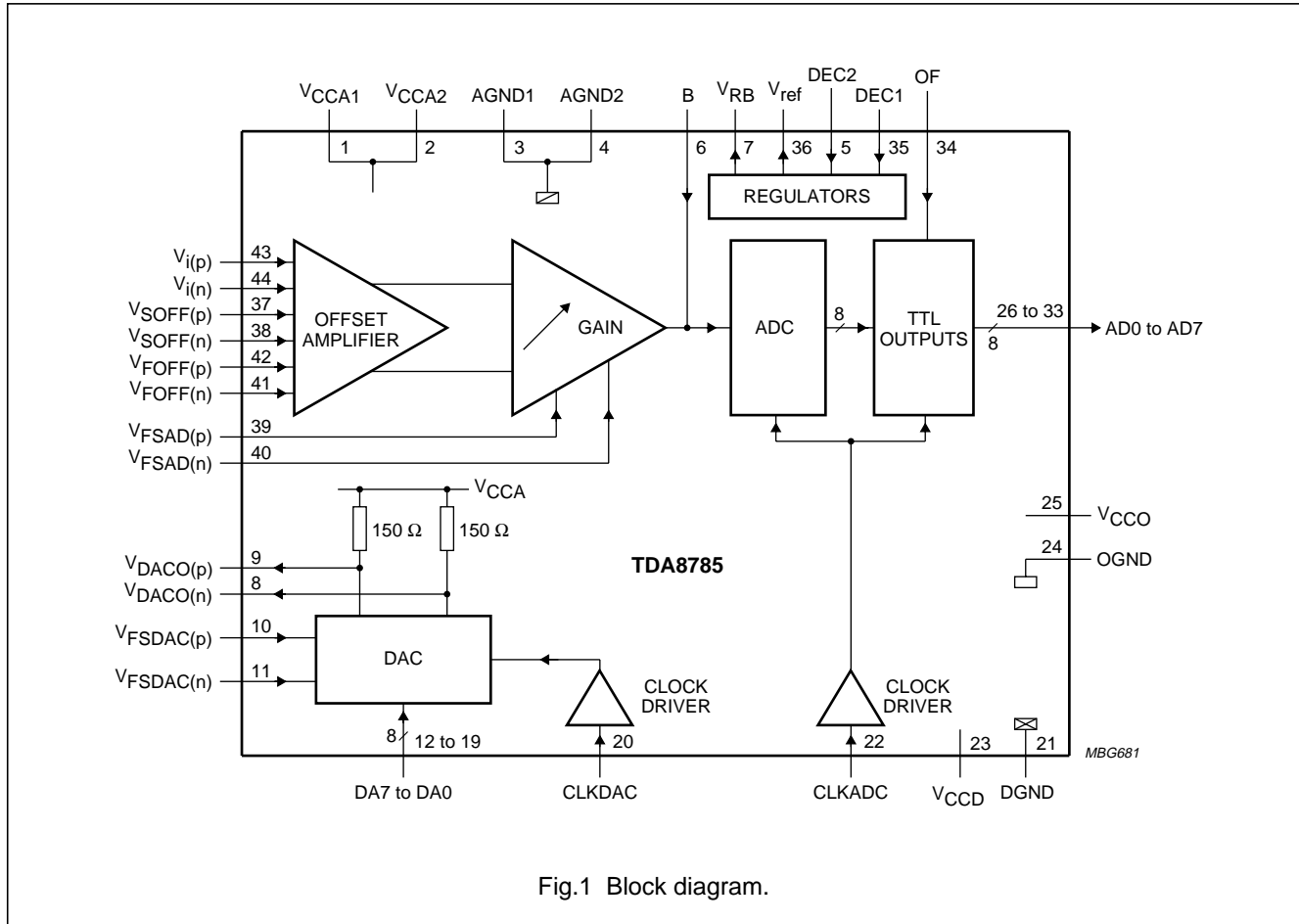


Fig.1 Block diagram.

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**PINNING**

SYMBOL	PIN	DESCRIPTION
V <sub>CCA1</sub>	1	analog supply voltage 1 (+5 V)
V <sub>CCA2</sub>	2	analog supply voltage 2 (+5 V)
AGND1	3	analog ground 1
AGND2	4	analog ground 2
DEC2	5	decoupling input 2
B	6	bandwidth adjustment node input
V <sub>RB</sub>	7	ADC reference voltage output bottom (decoupling)
V <sub>DACO(n)</sub>	8	DAC negative voltage output
V <sub>DACO(p)</sub>	9	DAC positive voltage output
V <sub>FSDAC(p)</sub>	10	DAC full-scale positive control voltage input
V <sub>FSDAC(n)</sub>	11	DAC full-scale negative control voltage input
DA7	12	DAC TTL input; bit 7 (MSB)
DA6	13	DAC TTL input; bit 6
DA5	14	DAC TTL input; bit 5
DA4	15	DAC TTL input; bit 4
DA3	16	DAC TTL input; bit 3
DA2	17	DAC TTL input; bit 2
DA1	18	DAC TTL input; bit 1
DA0	19	DAC TTL input; bit 0 (LSB)
CLKDAC	20	DAC clock input
DGND	21	digital ground
CLKADC	22	ADC clock input
V <sub>CCD</sub>	23	digital supply voltage (+5 V)

SYMBOL	PIN	DESCRIPTION
OGND	24	output ground
V <sub>CCO</sub>	25	output supply voltage (+5 V)
AD0	26	output data; bit 0 (LSB)
AD1	27	output data; bit 1
AD2	28	output data; bit 2
AD3	29	output data; bit 3
AD4	30	output data; bit 4
AD5	31	output data; bit 5
AD6	32	output data; bit 6
AD7	33	output data; bit 7 (MSB)
OF	34	output format input
DEC1	35	decoupling input 1
V <sub>ref</sub>	36	reference voltage output (2.75 V)
V <sub>SOFF(p)</sub>	37	slow offset amplifier positive voltage input
V <sub>SOFF(n)</sub>	38	slow offset amplifier negative voltage input
V <sub>FSAD(p)</sub>	39	gain control positive voltage input
V <sub>FSAD(n)</sub>	40	gain control negative voltage input
V <sub>FOFF(n)</sub>	41	fast offset amplifier negative voltage input
V <sub>FOFF(p)</sub>	42	fast offset amplifier positive voltage input
V <sub>i(p)</sub>	43	analog positive voltage input
V <sub>i(n)</sub>	44	analog negative voltage input

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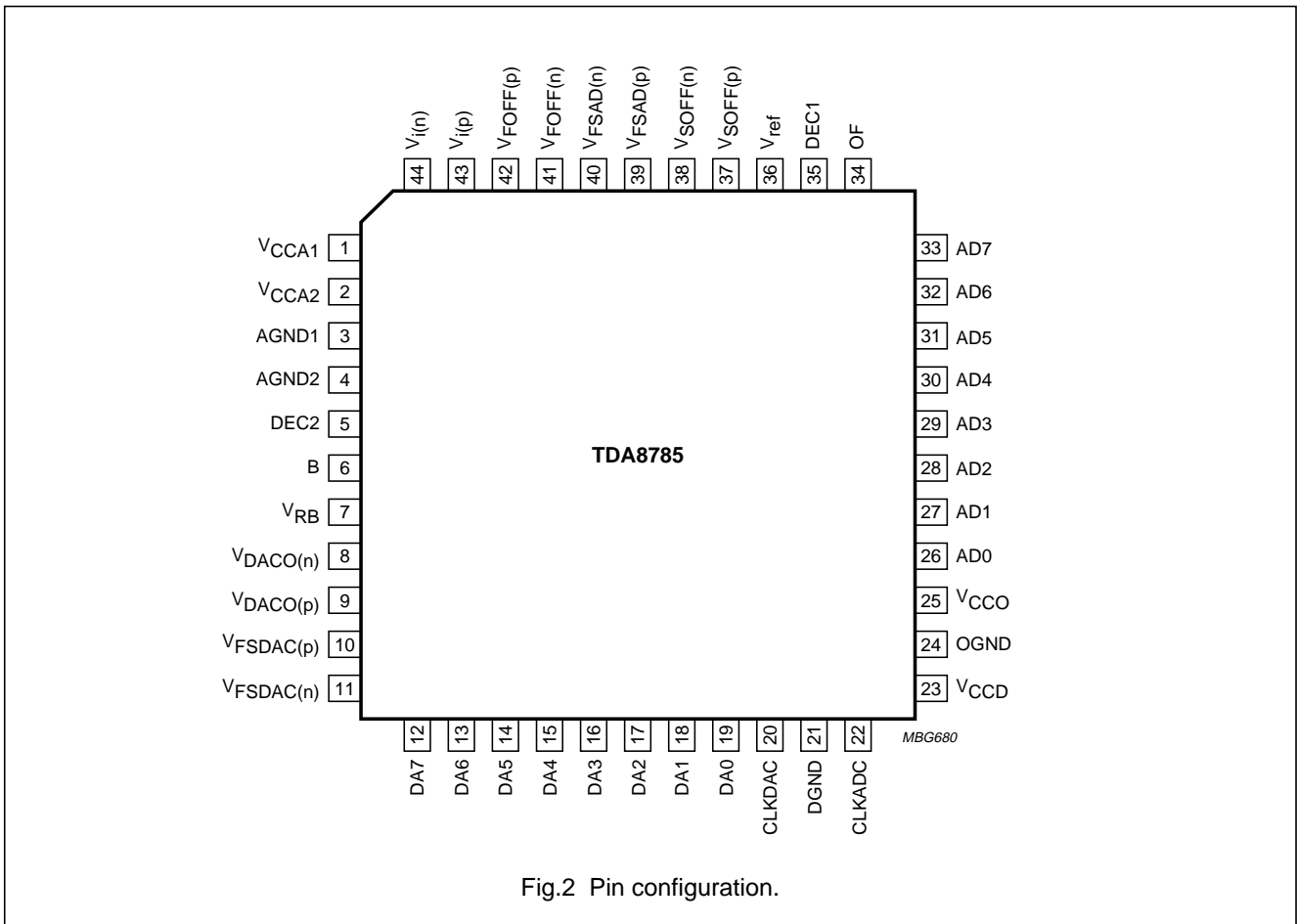


Fig.2 Pin configuration.

## 8-bit high-speed analog-to-digital converter with gain and offset controls

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### FUNCTIONAL DESCRIPTION

The TDA8785 is composed of an 8-bit ADC (30 Msps), a wide-band gain amplifier, an input offset amplifier and an 8-bit dynamic adjustment DAC.

#### Input signal

Two input pins are provided to apply a differential input signal with a wide range (100 to 1000 mV differential). It is also possible to apply a single signal by setting a DC voltage on one of the differential pins and supplying the signal to the other.

#### Controlled gain amplifier

The gain amplifier is used to adjust the wide input signal range to the fixed ADC input range of 1 V (p-p).

A large gain of 20 dB can be achieved with low-noise behaviour and a large bandwidth of 100 MHz to correctly amplify square type signals with step edges. Using pin 6, it is possible to reduce the internal bandwidth of the gain amplifier via an external capacitor and thus improve its noise behaviour. The gain amplifier is controlled via an external differential voltage (single input can also be applied).

#### Input offset amplifier and adjustment DAC

The Input offset amplifier contains two different control inputs (which can also be single):

- Slow offset control, for slow variation characteristics (e.g. temperature, supply voltage, etc.)
- Fast offset control, for correction related to the clock rate.

Slow offset control is carried out by an external voltage while fast offset control is digitally carried out via the internal 8-bit DAC with external connections of the respective pins  $V_{DACO(n)}$ ,  $V_{DACO(p)}$ ,  $V_{FOFF(n)}$  and  $V_{FOFF(p)}$ .

The internal 8-bit DAC operates at the ADC clock rate to allow dynamic corrections on the input signal chain based on the signal processing information carried out after the digital conversion. The output voltage amplitude of the DAC can be controlled via a different input voltage (which can also be single) in a range of  $\pm 25\%$  with a  $150\ \Omega$  DAC output load.

The DAC can also be used for the gain or the slow offset control with some external DC voltage adaptations and can be considered as a separate function of the ADC chain. The DAC can be used independently, for example as a video DAC.

#### 8-bit ADC

The 8-bit ADC converts a signal of 1 V (p-p) from the controlled gain amplifier into an 8-bit coded digital word at a maximum rate of 30 Msps. Its reference voltage is supplied by the general voltage regulator. The output data format can either be binary, two's complement or 3-state by selecting pin OF.

When all the differential inputs on the offset amplifier ( $V_{SOFF(p)}$ ,  $V_{SOFF(n)}$ ,  $V_{FOFF(n)}$ ,  $V_{FOFF(p)}$ ,  $V_{i(p)}$  and  $V_{i(n)}$ ) are at 0 V (equivalent to both inputs short-circuited), the output code of the ADC is code 8.

#### Internal voltage regulator

An internal voltage regulator provides all the references for the different blocks. A stable 2.75 V voltage reference output is provided for use in the application environment. One application is to connect all the slow control inputs ( $V_{FSDAC(p)}$ ,  $V_{FSDAC(n)}$ ,  $V_{SOFF(p)}$ ,  $V_{SOFF(n)}$ ,  $V_{FSAD(p)}$  and  $V_{FSAD(n)}$ ) to this reference, either to their two differential inputs to get the nominal settings or to one of the differential inputs to have easy single-input control.

All these control inputs have the same control range.

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## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CCA}$	analog supply voltage		-0.3	+7.0	V
$V_{CCD}$	digital supply voltage		-0.3	+7.0	V
$V_{CCO}$	output supply voltage		-0.3	+7.0	V
$\Delta V_{CC}$	supply voltage difference between $V_{CCA}$ and $V_{CCD}$		-1.0	+1.0	V
	$V_{CCD}$ and $V_{CCO}$		-1.0	+1.0	V
	$V_{CCA}$ and $V_{CCO}$		-1.0	+1.0	V
$V_I$	input voltage	referenced to AGND	-0.3	+7.0	V
$V_{clk(p-p)}$	clock input voltage for switching (peak-to-peak value)	referenced to DGND	-	$V_{CCD}$	V
$I_O$	output current		-	6	mA
$T_{stg}$	storage temperature		-55	+150	°C
$T_{amb}$	operating ambient temperature		0	70	°C
$T_j$	junction temperature		-	150	°C

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	75	K/W

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## CHARACTERISTICS

$V_{CCA1} = V_{CCA2} = V_{CCD} = V_{CCO} = 4.75$  to  $5.25$  V; AGND, DGND and OGND short-circuited together;  
 $V_{CCA}$  to  $V_{CCD} = V_{CCD}$  to  $V_{CCO} = V_{CCA}$  to  $V_{CCO} = -0.25$  to  $+0.25$  V;  $T_{amb} = 0$  to  $70$  °C;  
 typical values measured at  $V_{CCA} = V_{CCD} = V_{CCO} = 5$  V and  $T_{amb} = 25$  °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supplies</b>						
$V_{CCA1}$	analog supply voltage 1		4.75	5.0	5.25	V
$V_{CCA2}$	analog supply voltage 2		4.75	5.0	5.25	V
$V_{CCD}$	digital supply voltage		4.75	5.0	5.25	V
$V_{CCO}$	TTL output supply voltage		4.75	5.0	5.25	V
$I_{CCA}$	analog supply current		–	80	–	mA
$I_{CCD}$	digital supply current		–	30	–	mA
$I_{CCO}$	TTL output supply current		–	9	–	mA
<b>Reference voltages (pins <math>V_{ref}</math> and <math>V_{RB}</math>)</b>						
$V_{ref}$	output reference voltage		2.60	2.75	2.90	V
$V_{line}$	line regulation voltage	$V_{CCA} = 4.75$ to $5.25$ V	–	4	–	mV
$I_{LO}$	output load current		–1	–	–	mA
$V_{RB}$	reference voltage output bottom (decoupling)		–	$V_{CCA} - 2.5$	–	V
$V_{osB}$	offset voltage bottom	code 0 – $V_{RB}$	–	250	–	mV
$\Delta V_{ADC}$	ADC reference voltage difference	between code 0 and 255	–	1	–	V
<b>Analog inputs (pins <math>V_{I(p)}</math> and <math>V_{I(n)}</math>); see Table 1</b>						
$V_{i(p-p)}$	differential input voltage $V_{i(p)} - V_{i(n)}$ (peak-to-peak value)	0 dB gain	–	1000	–	mV
		20 dB gain	–	100	–	mV
$V_I$	DC input voltage		–	3.0	–	V
$I_i$	input current		–	10	–	$\mu$ A
$Z_i$	input impedance		–	20	–	k $\Omega$
$C_i$	input capacitance		–	1	–	pF
<b>Fast amplifier inputs (pins <math>V_{FOFF(p)}</math> and <math>V_{FOFF(n)}</math>); DC parameters</b>						
$V_{FOFF(p)}$	input voltage	0 dB gain	–	500	–	mV
		20 dB gain	–	50	–	mV
$V_{FOFF(n)}$	input voltage	0 dB gain	–	500	–	mV
		20 dB gain	–	50	–	mV
$V_I$	DC input voltage		–	$V_{CCA} - 0.25$	–	V
$I_i$	input current		–	10	–	$\mu$ A
$Z_i$	input impedance		–	20	–	k $\Omega$
$C_i$	input capacitance		–	1	–	pF



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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Slow offset amplifier inputs (pins <math>V_{SOFF(p)}</math> and <math>V_{SOFF(n)}</math>) gain amplifier at 0 dB; note 1</b>						
$V_{os}$	offset voltage at ADC input	$V_{SOFF(p)} = 2\text{ V};$ $V_{SOFF(n)} = 2.75\text{ V}$	–	–0.25	–	V
		$V_{SOFF(p)} = 2.75\text{ V};$ $V_{SOFF(n)} = 2.75\text{ V}$	–	0	–	V
		$V_{SOFF(p)} = 3.5\text{ V};$ $V_{SOFF(n)} = 2.75\text{ V}$	–	+0.25	–	V
$I_i$	input current		–	10	–	$\mu\text{A}$
<b>Offset reference code; <math>T_{amb} = 25\text{ }^\circ\text{C}</math></b>						
OFSRE	offset reference (ADC output code)	$V_{i(p)} = V_{i(n)};$	–	8	–	code
OFSER	offset reference error on code 8	$V_{FOFF(p)} = V_{FOFF(n)};$ $V_{SOFF(p)} = V_{SOFF(n)};$ amplifier gain set at 0 dB	tbf	0	tbf	code
<b>Gain control inputs (pins <math>V_{FSAD(p)}</math> and <math>V_{FSAD(n)}</math>); see Fig.7</b>						
$G_{v(min)}$	minimum voltage gain	$V_{FSAD(p)} = 2\text{ V};$ $V_{FSAD(n)} = 2.75\text{ V}$	–	–	0	dB
$G_{v(max)}$	maximum voltage gain	$V_{FSAD(p)} = 3.5\text{ V};$ $V_{FSAD(n)} = 2.75\text{ V}$	20	–	–	dB
$I_i$	input current		–	10	–	$\mu\text{A}$
<b>DAC full-scale control inputs (pins <math>V_{FSDAC(p)}</math> and <math>V_{FSDAC(n)}</math>) 150 <math>\Omega</math> output load on pins <math>V_{DACO(p)}</math> and <math>V_{DACO(n)}</math>; see Table 3</b>						
$V_{DACO(n)}$	DAC output voltage (pin 8)	code 0 at DAC inputs	–	$V_{CCA}$	–	V
		code 255 at DAC inputs; $V_{FSDAC(p)} = 2\text{ V};$ $V_{FSDAC(n)} = 2.75\text{ V}$	–	$V_{CCA} - 0.4$	–	V
		code 255 at DAC inputs; $V_{FSDAC(p)} = 2.75\text{ V};$ $V_{FSDAC(n)} = 2.75\text{ V}$	–	$V_{CCA} - 0.5$	–	V
		code 255 at DAC inputs; $V_{FSDAC(p)} = 3.5\text{ V};$ $V_{FSDAC(n)} = 2.75\text{ V}$	–	$V_{CCA} - 0.6$	–	V
$I_i$	input current		–	2	–	$\mu\text{A}$
<b>Bandwidth adjustment node input (pin B); see Fig.6</b>						
$Z_i$	input impedance		–	500	–	$\Omega$
<b>8-bit DAC; <math>f_{clk} = 30\text{ MHz}</math>, ramp input; <math>T_{amb} = 25\text{ }^\circ\text{C}</math></b>						
$Z_o$	output impedance		–	150	–	$\Omega$
INL	integral non-linearity		–	$\pm 0.4$	tbf	LSB
DNL	differential non-linearity		–	$\pm 0.4$	tbf	LSB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Digital inputs (pins CLKDAC, CLKADC and DA7 to DA0)</b>						
V <sub>IL</sub>	LOW level input voltage		0	–	0.8	V
V <sub>IH</sub>	HIGH level input voltage		2.0	–	V <sub>CCD</sub>	V
I <sub>IL</sub>	LOW level input current	V <sub>clk</sub> = 0.4 V	–400	–	–	μA
I <sub>IH</sub>	HIGH level input current	V <sub>clk</sub> = 2.7 V	–	–	100	μA
Z <sub>i</sub>	input impedance	f <sub>clk</sub> = 10 MHz	–	4	–	kΩ
C <sub>i</sub>	input capacitance	f <sub>clk</sub> = 10 MHz	–	4.5	–	pF
<b>ADC output format (pin OF); see Table 2</b>						
V <sub>IL</sub>	LOW level input voltage		0	–	0.2	V
V <sub>IH</sub>	HIGH level input voltage		2.6	–	V <sub>CCD</sub>	V
V <sub>I</sub>	input voltage in high impedance state		–	1.15	–	V
I <sub>IL</sub>	LOW level input current	V <sub>clk</sub> = 0.4 V	–370	–300	–	μA
I <sub>IH</sub>	HIGH level input current	V <sub>clk</sub> = 2.7 V	–	300	450	μA
<b>ADC digital outputs</b>						
V <sub>OL</sub>	LOW level output voltage	I <sub>OL</sub> = 2 mA	0	–	0.6	V
V <sub>OH</sub>	HIGH level output voltage	I <sub>OH</sub> = –0.4 mA	2.4	–	V <sub>CCO</sub>	V
<b>ADC and DAC switching; see Fig.4</b>						
f <sub>clk(max)</sub>	maximum clock frequency	note 2	30	–	–	MHz
t <sub>CPH</sub>	clock pulse width HIGH		12	–	–	ns
t <sub>CPL</sub>	clock pulse width LOW		12	–	–	ns
<b>Analog processing; note 3</b>						
INL	integral non-linearity	ramp input (full scale); 0 to 20 dB gain	–	±0.7	tbf	LSB
DNL	differential non-linearity	ramp input (full scale); 0 to 20 dB gain	–	±0.4	tbf	LSB
S/N	signal-to-noise ratio (without harmonics)	f <sub>i</sub> = 4.43 MHz 0 dB gain 10 dB gain 20 dB gain	–	47 45 43	–	dB dB dB
B	bandwidth	–3 dB	–	100	–	MHz
t <sub>s</sub>	settling time	note 4	–	2	–	code

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Timing</b>						
ADC DIGITAL OUTPUTS ( $C_L = 15$ pF)						
$t_{ds}$	sampling delay time		–	1.5	–	ns
$t_h$	output hold time		7	–	–	ns
$t_d$	output delay time		–	–	16	ns
DAC OUTPUTS (PINS $V_{DACO(p)}$ AND $V_{DACO(n)}$ )						
$t_{SU; DAT}$	data set-up time	note 5	–0.3	–	–	ns
$t_{HD; DAT}$	data hold time	note 5	–	–	2	ns
$t_s$	DAC settling time (1% accuracy)	$R_L = 150 \Omega$ ; $C_L = 15$ pF	–	8	–	ns
3-STATE OUTPUT DELAY TIMES (see Fig.5)						
$t_{dZH}$	enable HIGH		–	12	14	ns
$t_{dZL}$	enable LOW		–	10	12	ns
$t_{dHZ}$	disable HIGH		–	58	62	ns
$t_{dLZ}$	disable LOW		–	70	74	ns

**Notes**

- $V_{os}$  is proportional to the amplifier gain. For instance,  $V_{os}$  at 20 dB is the one indicated at 0 dB multiplied by 10.
- It is recommended that the rise and fall times of the clock are  $>1$  ns. In addition a good layout for the digital and analog grounds is recommended.
- Analog processing from signal inputs or fast offset amplifier inputs to ADC digital output;  $f_{clk} = 30$  MHz; no external filtering on pin 6 (B).
- Settling time is the number of code variations at the ADC output, after one clock period settling. A full-scale jump is applied at the DAC inputs, with the DAC output (square signal) connected to the fast offset amplifier input. ADC and DAC clock signals (CLKADC and CLKDAC) are in phase.
- The data set-up time ( $t_{SU; DAT}$ ) is the minimum period preceding the rising edge of the clock, that the input data must be stable in order to be correctly registered. A negative set-up time indicates that the data may be initiated after the rising edge and still be recognized. The data set hold time ( $t_{HD; DAT}$ ) is the minimum period following the rising edge of the clock, that the input data must be stable in order to be correctly registered. A negative hold time indicates that the data may be released prior to the rising edge and still be recognized.

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**Table 1** Output coding and input voltage (typical values; referenced to AGND,  $V_{i(p)} - V_{i(n)} = 1$  V (p-p), 0 dB gain, no offset correction)

STEP	$V_{i(p)} - V_{i(n)}$	BINARY OUTPUT BITS								TWO'S COMPLEMENT OUTPUT BITS							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Underflow	$<-0.032$	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	$-0.032$	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	–	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
8	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254	–	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	0.968	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
Overflow	$>0.968$	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

**Table 2** OF input coding

OF	AD0 to AD7
0	active, two's complement
1	high impedance
open circuit <sup>(1)</sup>	active, binary

### Note

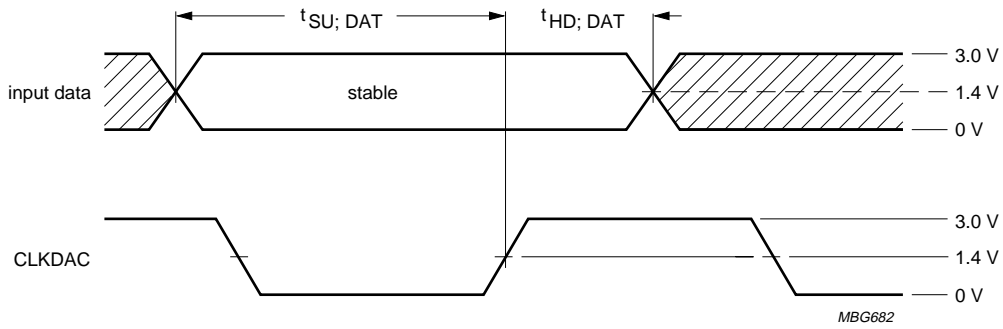
- Use  $C \geq 10$  pF to DGND.

**Table 3** Input coding and DAC output voltages (typical values; referenced to  $V_{CCA}$  regardless of the offset voltage);  
 $V_{FSDAC(p)} = V_{FSDAC(n)}$

CODE	BINARY INPUT DATA								DAC OUTPUT VOLTAGES (V)			
	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	$Z_L = 10$ k $\Omega$		$Z_L = 150$ $\Omega$	
									$V_{DACO(p)}$	$V_{DACO(n)}$	$V_{DACO(p)}$	$V_{DACO(n)}$
0	0	0	0	0	0	0	0	0	-1.0	0	-0.5	0
1	0	0	0	0	0	0	0	1	–	–	–	–
.	.	.	.	.	.	.	.	.	.	.	.	.
128	1	0	0	0	0	0	0	0	-0.5	-0.5	-0.25	-0.25
.	.	.	.	.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0	–	–	–	–
255	1	1	1	1	1	1	1	1	0	-1.0	0	-0.5

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The shaded areas indicate when the input data may change and be correctly registered. Data input update must be completed within 0.3 ns, after the first rising edge of the clock ( $t_{SU; DAT}$  is negative; -0.3 ns). Data must be held at least 2 ns after the rising edge ( $t_{HD; DAT} = +2$  ns).

Fig.3 Data set-up and hold times (DAC).

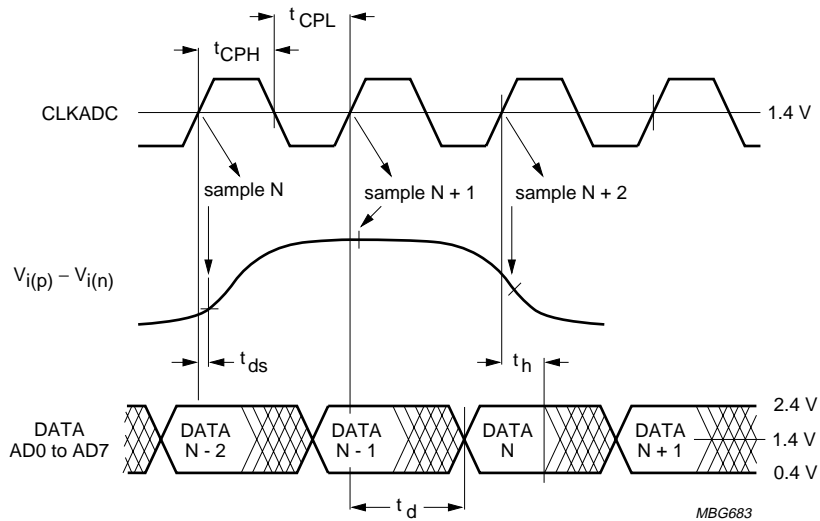


Fig.4 Timing diagram

8-bit high-speed analog-to-digital converter  
with gain and offset controls

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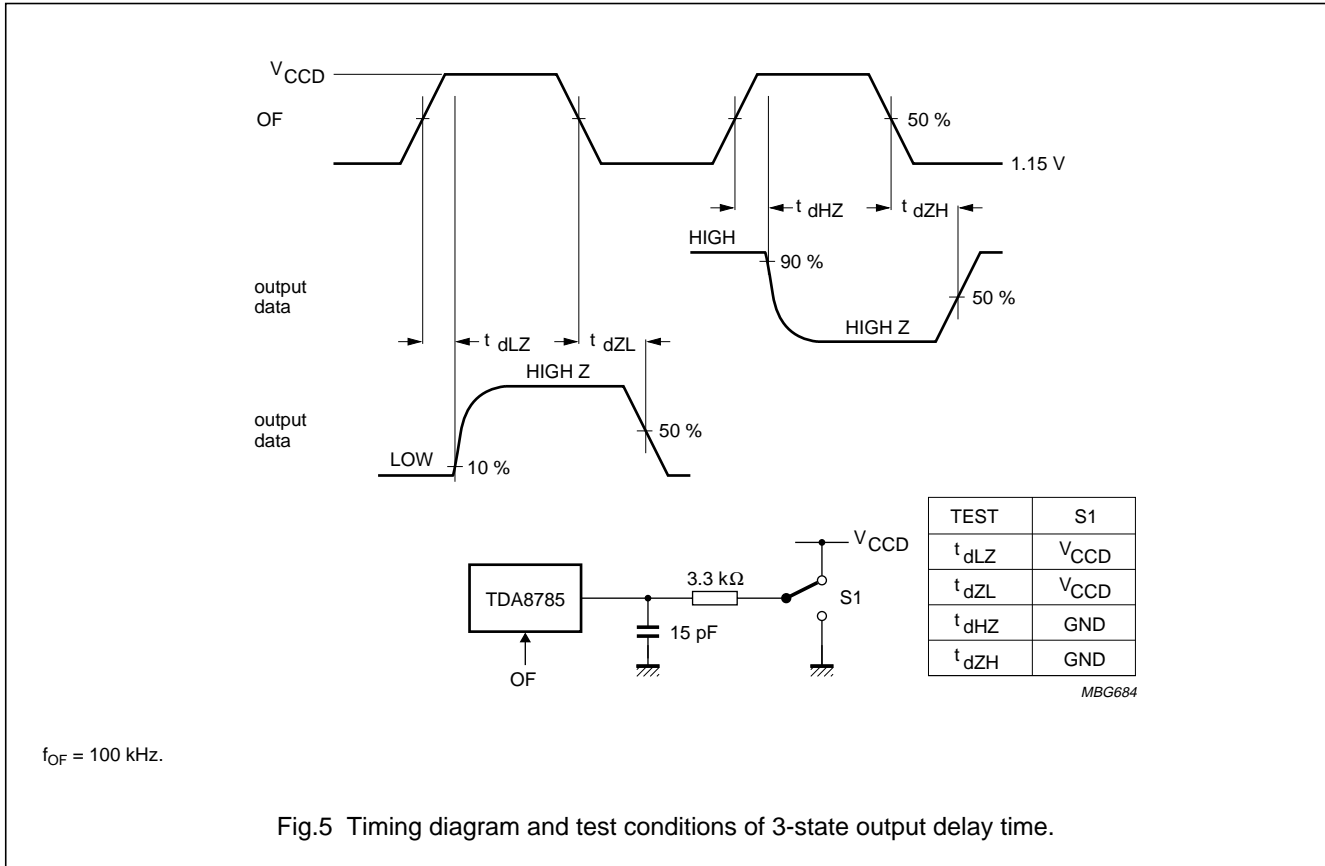
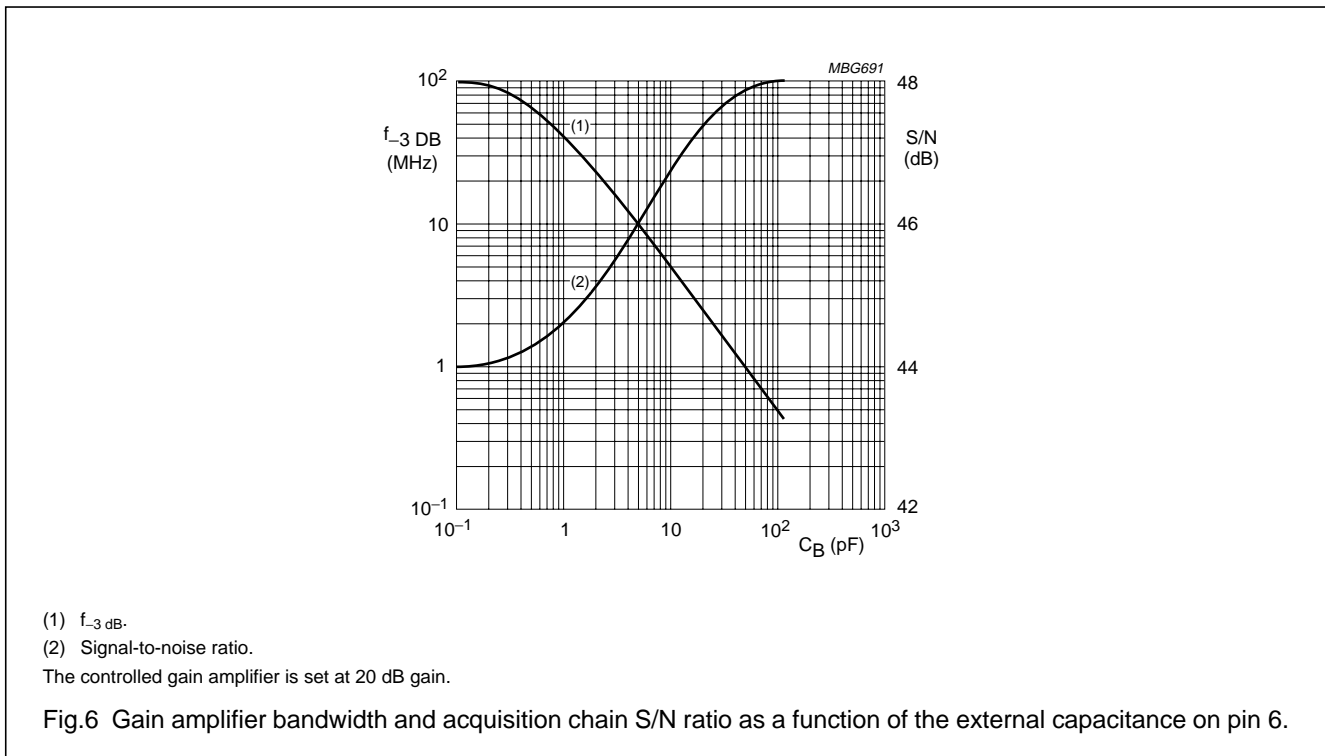


Fig.5 Timing diagram and test conditions of 3-state output delay time.



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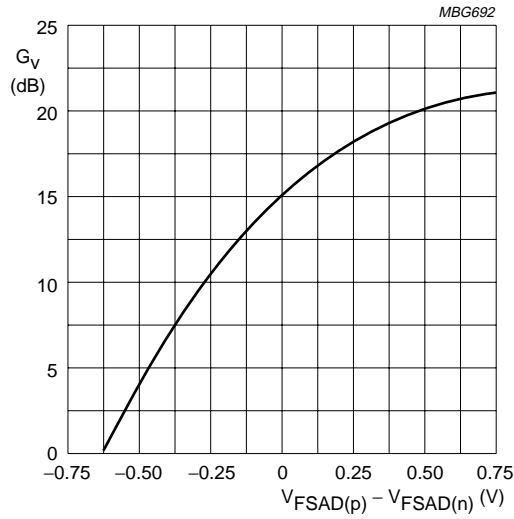
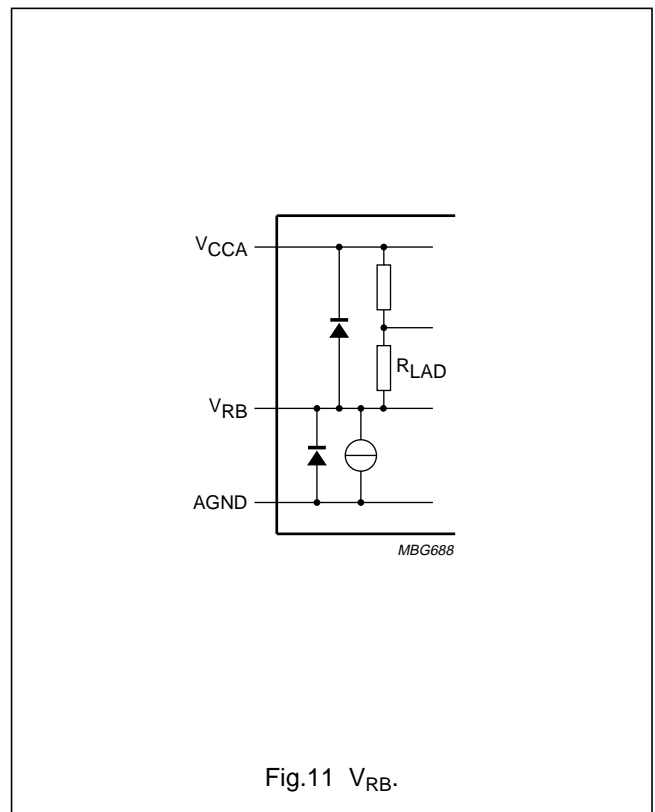
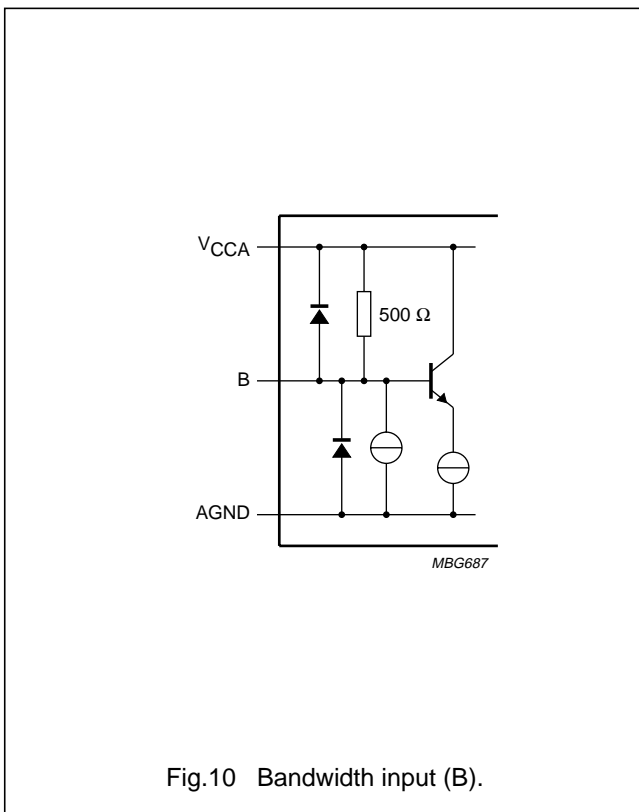
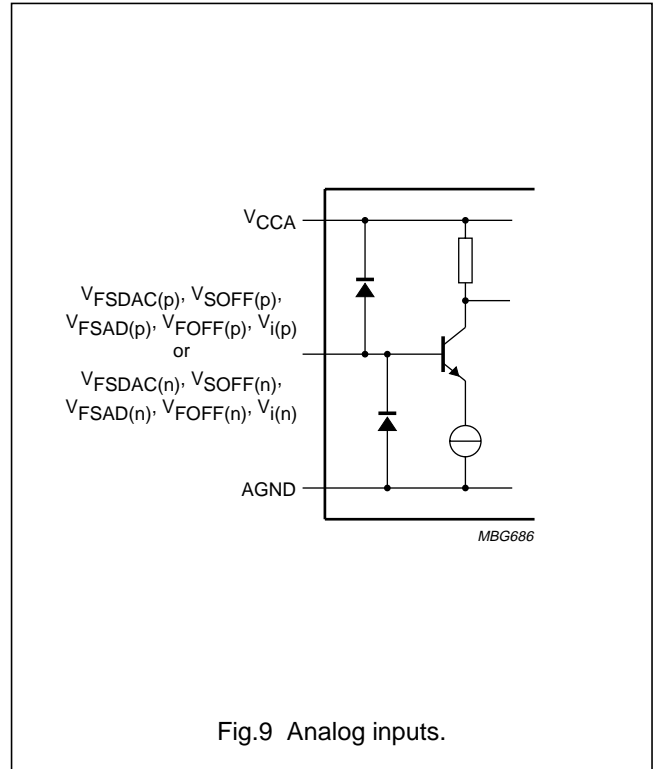
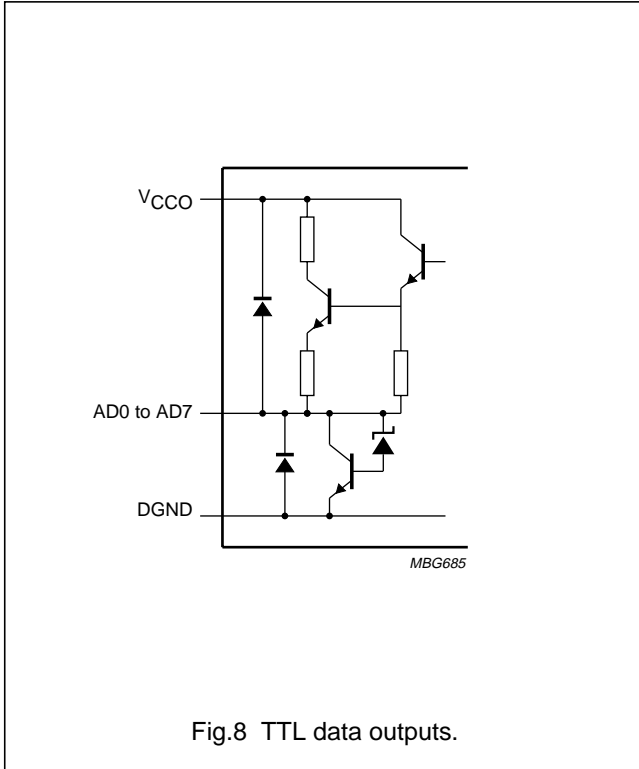


Fig.7 Typical amplifier gain ( $G_V$ ) as a function of the differential input voltage;  $V_{FSAD(p)} - V_{FSAD(n)}$ .

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## INTERNAL PIN CONFIGURATIONS





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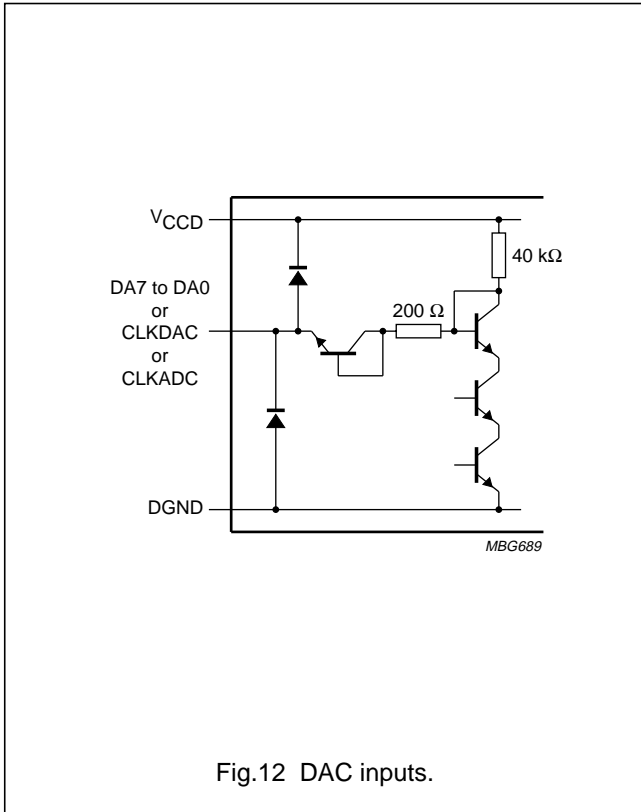


Fig.12 DAC inputs.

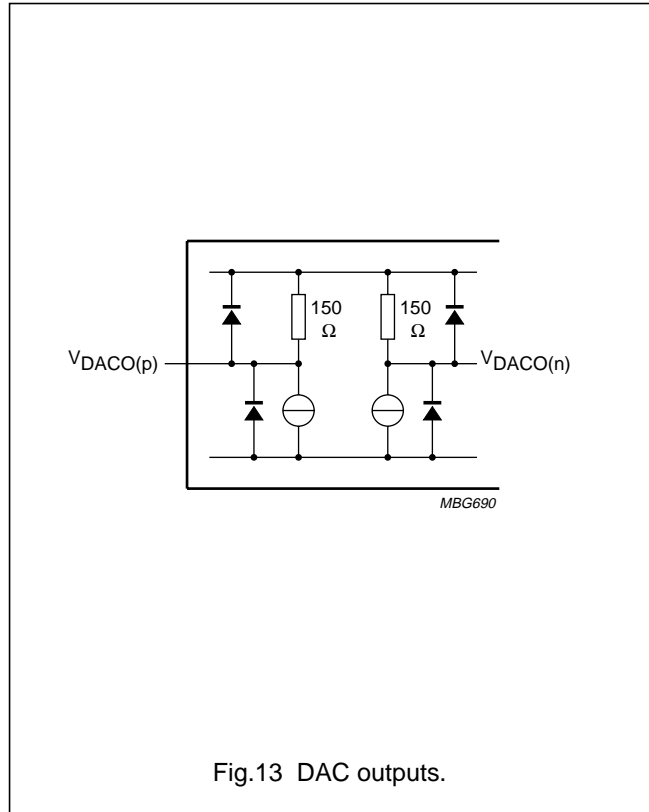


Fig.13 DAC outputs.

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## APPLICATION INFORMATION

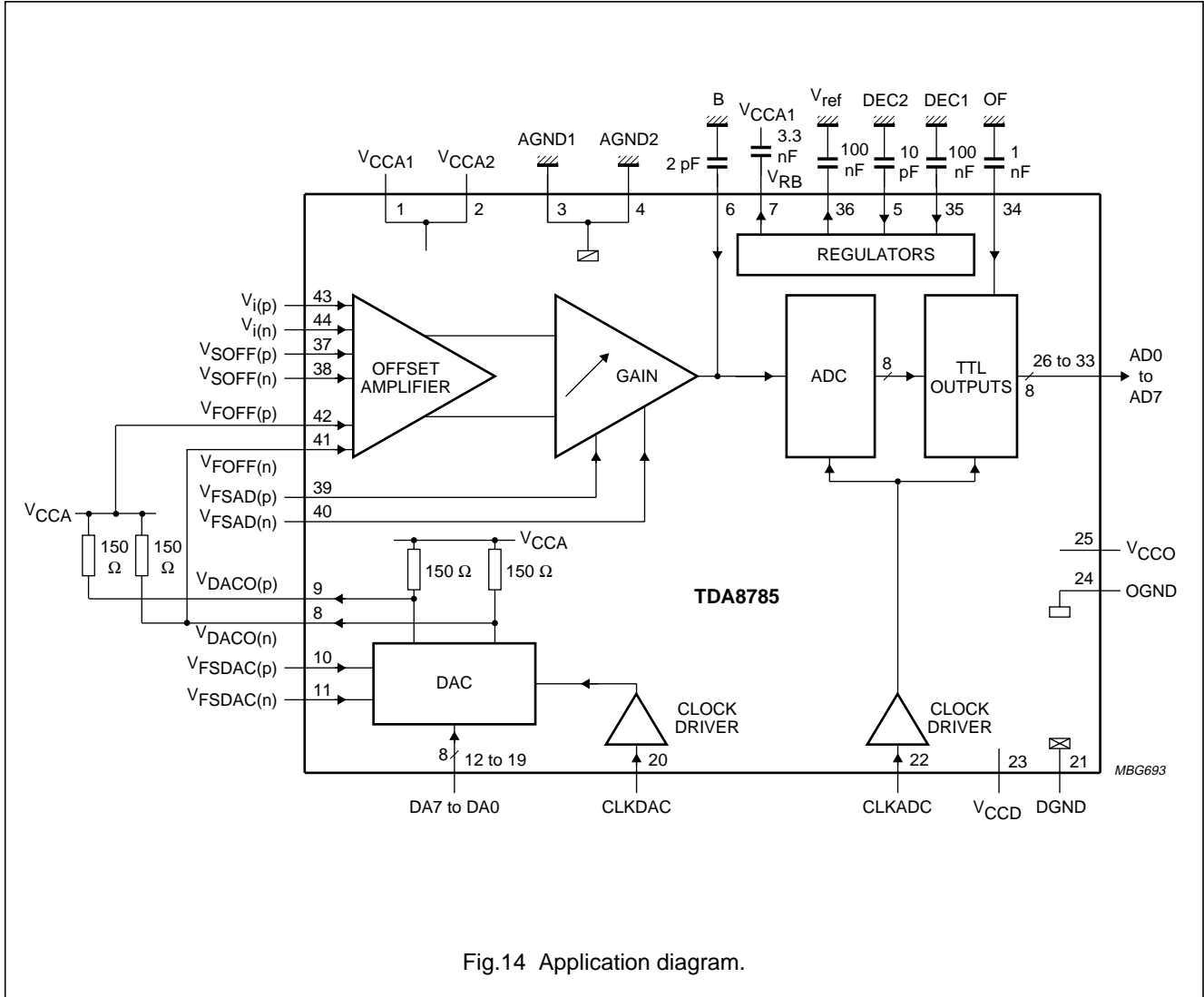


Fig.14 Application diagram.

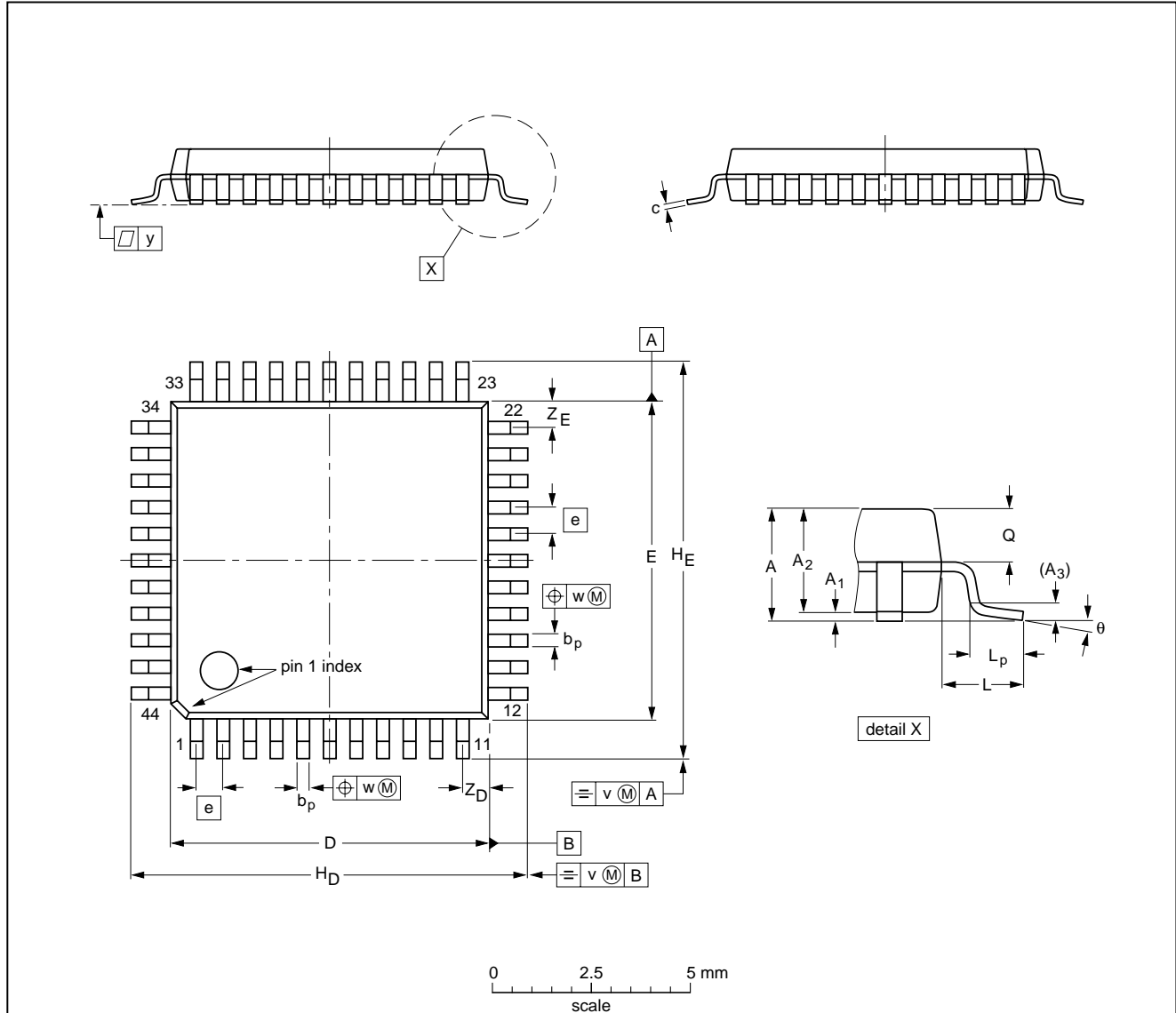
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## PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm

SOT307-2



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>D</sub>	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sub>D</sub> <sup>(1)</sup>	Z <sub>E</sub> <sup>(1)</sup>	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.85 0.75	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						92-11-17 95-02-04

## 8-bit high-speed analog-to-digital converter with gain and offset controls

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### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

#### Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our "Quality Reference Handbook" (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

#### Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

**If wave soldering cannot be avoided, the following conditions must be observed:**

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

**Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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## DEFINITIONS

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

## LIFE SUPPORT APPLICATIONS

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**NOTES**

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**NOTES**

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